IN THE CLAIMS

What is claimed is:

1. A method of forming a microelectronic structure comprising:

forming and patterning a deep uv resist layer on a substrate; and

etching the substrate in a plasma generated from a gas comprising a carbon to fluorine ratio from about 1:1 to about 2:3 to form substantially vertical sidewalls in the deep uv resist layer.

2. The method of claim 1 wherein forming and patterning the deep uv resist layer comprises forming a deep uv resist layer and exposing at least a portion of the deep uv resist layer to a light with a wavelength of about 200 nanometers or less.

3. The method of claim 1 wherein etching the deep uv resist layer and the substrate in the plasma to form substantially vertical sidewalls comprises etching the substrate in the plasma to form a polymer on the sidewalls of the deep uv resist layer that substantially prevents the deep uv resist layer from being etched.

4. The method of claim 1 wherein forming the deep uv resist layer

comprises forming the deep uv resist layer wherein the deep uv resist layer comprises a pre-etch sidewall angle that is substantially the same as a post etch sidewall angle.

5. The method of claim 1 further comprising etching the substrate in a plasma generated from a gas comprising C_4F_6, and a pressure from about 15 to about 100 millitorr.

6. The method of claim 5 further comprising etching the substrate with a power from about 1000 to about 4000 Watts, a C_4F_6 gas flow from about 10 to about 50 sccm, an argon flow from about 100 to about 1000 sccm, and a nitrogen flow from about 50 to 100 sccm.

7. The method of claim 1 wherein forming and patterning the deep uv resist layer on a substrate comprises forming a deep uv resist layer on a sacrificial light absorbing layer disposed on a dielectric layer.

8. The method of claim 7 wherein etching the sacrificial light absorbing layer disposed on the dielectric layer in a plasma generated from a gas comprising a carbon to fluorine ratio from about 1:1 to about 2:3 comprises:

substantially etching the sacrificial light absorbing layer and then substantially etching the underlying dielectric layer by utilizing a plasma generated from a gas comprising C_4F_6.

9. The method of claim 8 further comprising substantially etching the sacrificial light absorbing layer and then substantially etching the underlying dielectric layer in a pressure from about 15 to about 100 millitorr and a power from about 1000 to about 4000 Watts.

10. The method of claim 8 further comprising substantially etching the sacrificial light absorbing layer and then substantially etching the underlying dielectric layer in a C_4F_6 gas flow from about 10 to about 50 sccm, an argon flow from about 100 to about 1000 sccm, and a nitrogen flow from about 50 to 100 sccm.

11. The method of claim 1 wherein etching the substrate in the plasma to form a substantially vertical sidewall in the deep uv resist layer comprises etching the substrate in the plasma to form a sidewall angle that is between about 86 and about 90 degrees.

12. The method of claim 1 wherein forming and patterning the deep uv

resist layer on a substrate comprises forming and patterning the deep uv resist layer on a substrate, wherein the deep uv resist layer comprises an acrylic polymer.

13. A method of forming a microelectronic structure comprising:

forming and patterning a deep uv resist layer on a sacrificial light absorbing layer disposed on a dielectric layer; and

etching the sacrificial light absorbing layer and the dielectric layer in a plasma generated from a gas comprising a carbon to fluorine ratio that is between about 1:1 to about 2:3, at an etch rate from about 80 to about 120 times faster than the etch rate of the deep uv resist layer in the plasma.

14. The method of claim 13 further comprising etching the sacrificial light absorbing layer and the dielectric layer in a plasma generated from a gas comprising C_4F_6.

15. The method of claim 14 further comprising etching the sacrificial light absorbing layer in a pressure from about 40 to about 60 millitorr, and then etching the dielectric layer in a pressure from about 80 to about 120 millitorr.

16. The method of claim 15 further comprising:

etching the sacrificial light absorbing layer in a C_4F_6 gas flow from about 14 to about 20 sccm, an argon flow from about 300 to about 500 sccm, and a nitrogen flow from about 200 to 400 sccm; and

etching the dielectric layer in a C_4F_6 gas flow from about 10 to about 14 sccm, an argon flow from about 280 to about 350 sccm, and a nitrogen flow from about 25 to 40 sccm.

17. A method of forming a microelectronic structure comprising:

forming a deep uv resist layer on a sacrificial light absorbing layer that is disposed on a dielectric layer;

patterning a portion of the sacrificial light absorbing layer to define a trench;

forming a bottom width of the trench, wherein the ratio of the bottom width to a top width of the trench is about 1:1 by:

etching the sacrificial light absorbing layer in a plasma generated from a gas comprising a carbon to fluorine ratio that is between about 1:1 to about 2:3; and

etching the dielectric layer in a plasma generated from a gas comprising a carbon to fluorine ratio that is between about 1:1 to about 2:3.

18. The method of claim 17 wherein etching the sacrificial light absorbing

layer in a plasma generated from a gas comprising a carbon to fluorine ratio that is between about 1:1 to about 2:3, comprises etching the sacrificial light absorbing layer in a plasma generated from a gas comprising C_4F_6,

19. The method of claim 18 further comprising etching the sacrificial light absorbing layer in a pressure from about 40 to about 60 millitorr and a power from about 1000 to about 4000 Watts,

20. The method of claim 19 further comprising etching the sacrificial light absorbing material in a C_4F_6 gas flow from about 10 to about 20 sccm, an argon flow from about 400 to about 500 sccm, and a nitrogen flow from about 200 to about 400 sccm.

21. The method of claim 17 wherein etching the dielectric layer in a plasma generated from a gas comprising a carbon to fluorine ratio gas that is between about 1:1 to about 2:3 comprises etching the dielectric layer in a plasma generated from a gas comprising C_4F_6, a pressure from about 90 to about 110 millitorr, a C_4F_6 gas flow from about 10 to about 15 sccm, an argon flow from about 250 to about 350 sccm and a nitrogen flow from about 20 to about 50 sccm.

22. An intermediate product comprising:

a trench in a substrate, wherein a deep uv resist layer is disposed on a first surface of the trench, and wherein the deep uv resist layer comprises a sidewall that is substantially vertical and comprises a polymer on the sidewall; and

a bottom width of the trench wherein the ratio of the bottom width to a top width of the trench is about 1:1.

23. The intermediate product of claim 22 wherein the deep uv resist layer comprises a sidewall angle that is from about 85 to about 90 degrees.

24. The intermediate product of claim 22 wherein the bottom width of the trench is from about 80 to about 90 nm.

25. The intermediate product of claim 22 wherein the deep uv resist layer is between about 2,100 to about 3,000 angstroms in thickness.

26. The intermediate product of claim 22 further comprising a trench sidewall, wherein the trench sidewall comprises has a low k dielectric layer that comprises a dielectric constant below about 4.

27. The intermediate product of claim 22 wherein the low k dielectric layer comprises a material selected from the group consisting of carbon doped

oxide, organic polymers such as a polyimide, parylene, polyarylether, organo-silicone, polynaphthalene, polyquinoline, or copolymers thereof, spin on glass materials, either doped or undoped, and porous materials such as xerogels and others that include templated pores.